Method for Identification of Faulty or Weak Functional Logic Elements under Simulated Extreme Operating Conditions

ABSTRACT OF THE DISCLOSURE

A method for testing a circuit is provided. The method includes providing a normal internal clock signal for use in accessing functional logic, where the functional logic has access to redundant functional logic during normal operation. The method then applies a stress clock signal to the functional logic, and each pulse of the stress clock signal is of a shorter duration than each pulse of the normal internal clock signal. Based on the applied stress clock signal, the method identifies logic elements of the functional logic that fail to operate as intended.